Addressing High Frequency Challenges for Burn-in Requiring LVDS

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Contents

- Introduction
- Addressing Various LVDS Issues
- Design of Experiments
- Results and Discussion
- Recommendation
- Acknowledgement

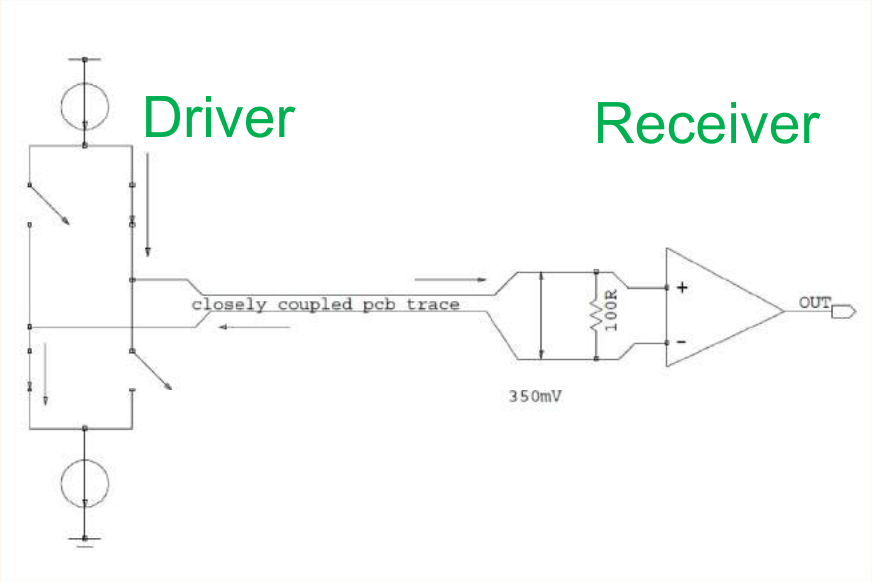
Introduction

- LVDS = Low Voltage Differential Signaling
- It is also known as TIA/EIA-644, a standard entitled “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits”
  - *TIA = Telecommunication Industry Association*
  - *EIA = Electronic Industries Alliance*

Introduction

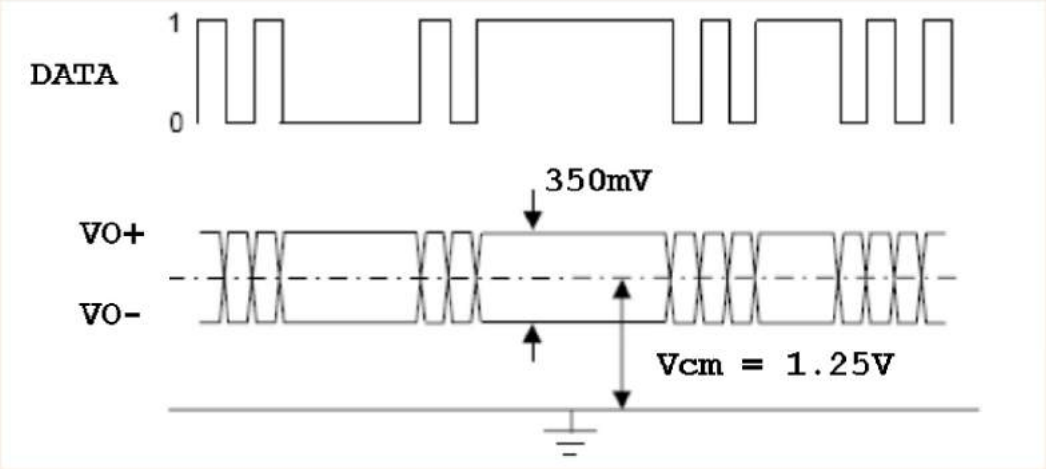
- LVDS is a low voltage, low power, differential technology used primarily for point-to-point and multi-drop driving applications

Introduction



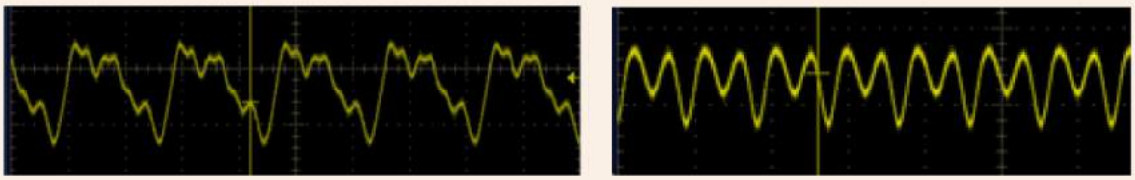
LVDS

Introduction



LVDS

Introduction



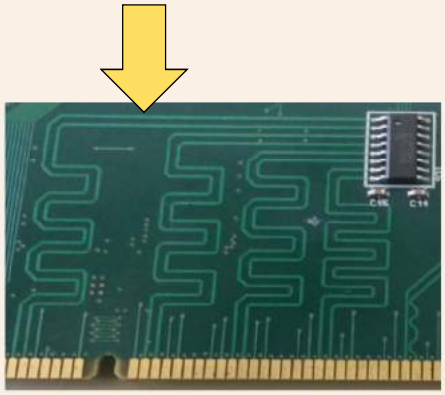
Sample scope shots of 27 MHz single-ended signals captured on burn-in boards

- **Harmonic Distortion**
- **Doubled Frequency**
- **Attenuation beyond 100 MHz**

Addressing Various LVDS Issues

- LVDS, a pair of PCB traces

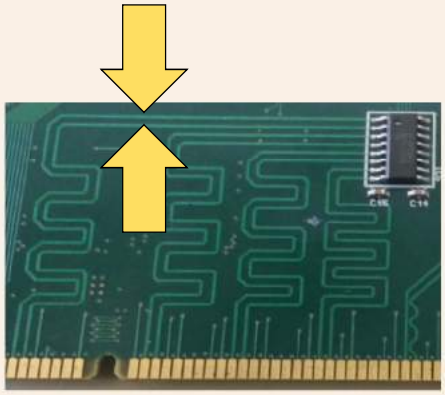
  1) Differential traces should be as close as possible after leaving the driver output



Addressing Various LVDS Issues

- LVDS, a pair of PCB traces

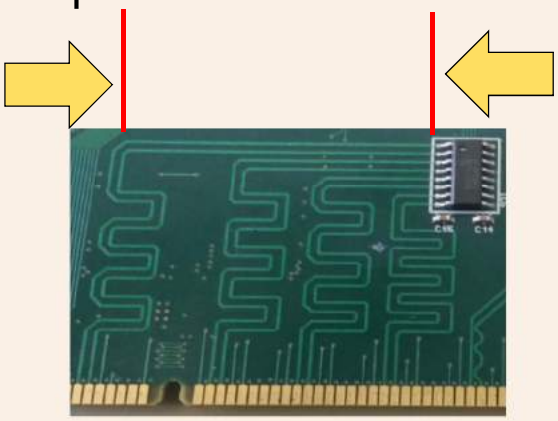
  2) Distances between differential LVDS signals should remain constant on the entire length of the traces



Addressing Various LVDS Issues

- LVDS, a pair of PCB traces

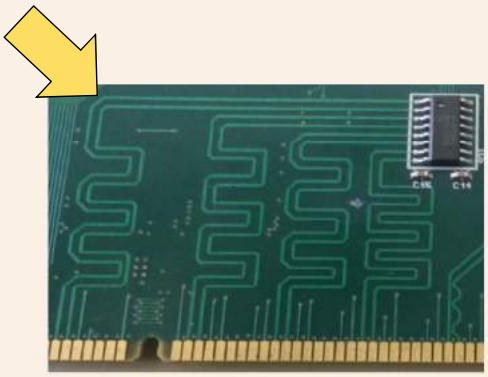
  3) Electrical lengths should be the same between differential pairs



Addressing Various LVDS Issues

- LVDS, a pair of PCB traces

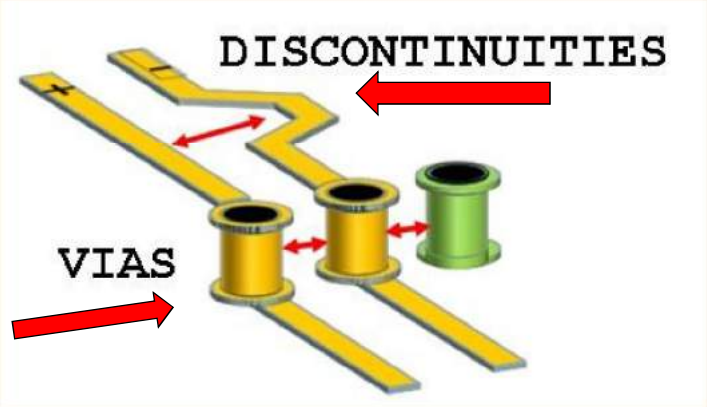
  4) Arcs or 45° traces for each turn of traces



Addressing Various LVDS Issues

- LVDS, a pair of PCB traces

  5) Minimize number of vias and other discontinuities



Addressing Various LVDS Issues

- LVDS, a pair of PCB traces

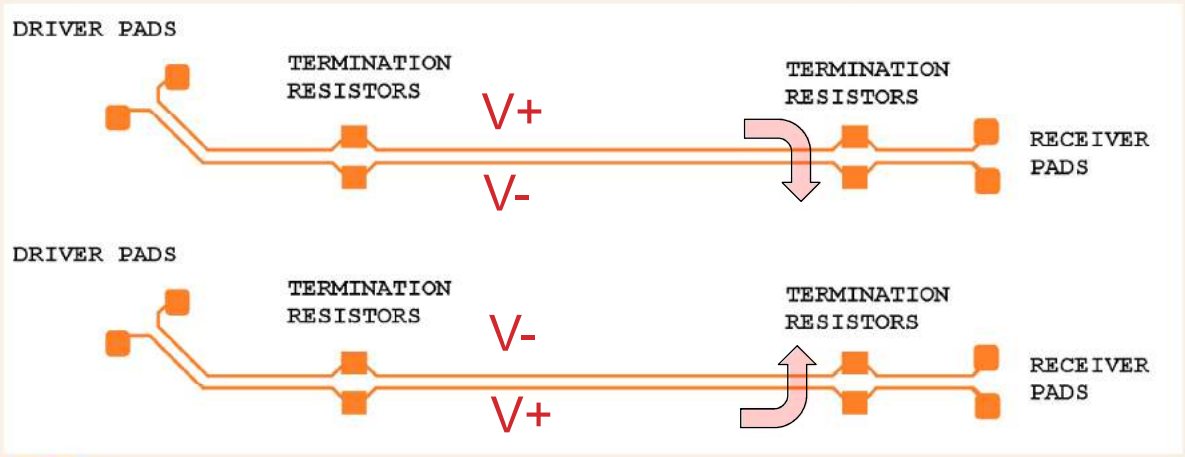
  6) Parasitic loading (e.g. capacitance) must be present in equal amounts to each line

"Symmetry is KEY"

Addressing Various LVDS Issues

- Electromagnetic Interference

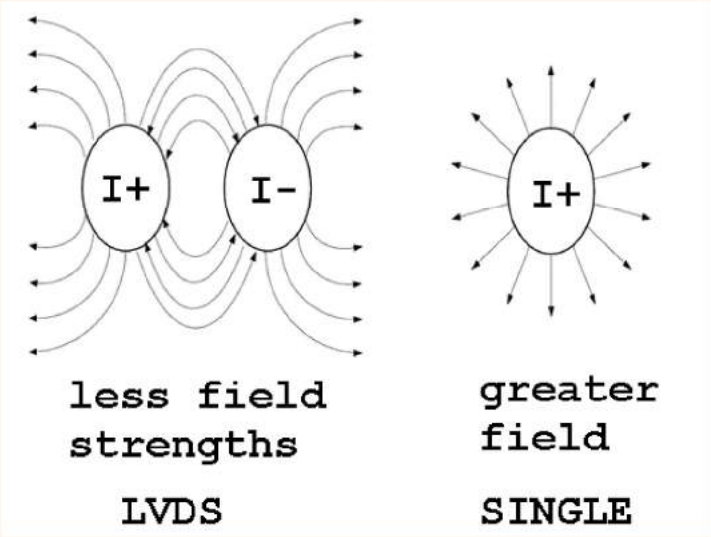
  When the driver switches from logic high to logic low or vice versa, it changes the direction of current flow on the termination resistor.



Addressing Various LVDS Issues

- Electromagnetic Interference (EMI)

  LVDS generates lesser EMI

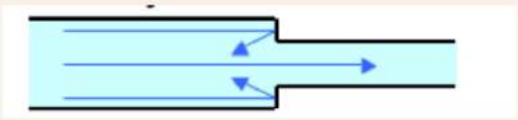


Addressing Various LVDS Issues

- Impedance Matching

Without reflection

Good Impedance Matching



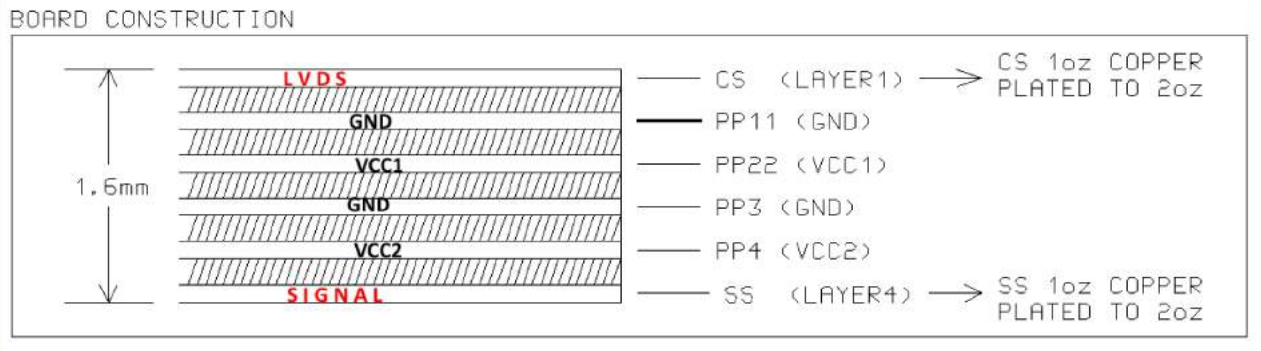
With reflection

Improper Impedance Matching

Addressing Various LVDS Issues

- Crosstalk

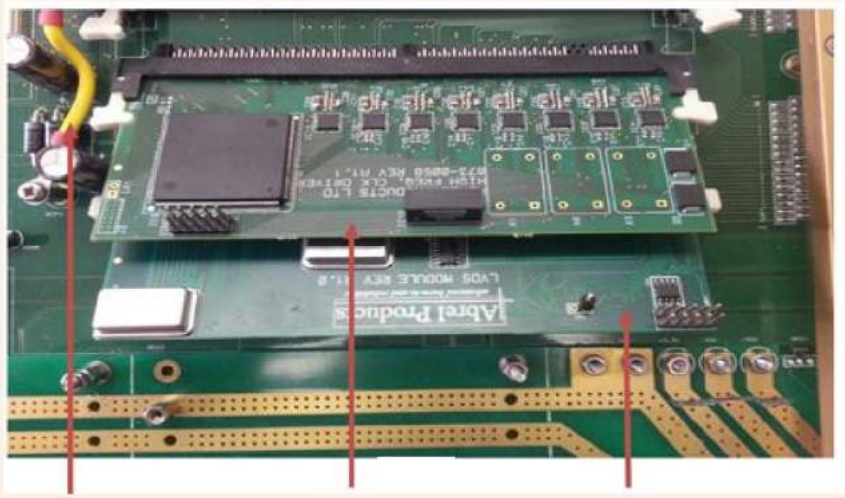
  To isolate LVDS signal layers from single-ended, POWER and GND planes are placed in between



Addressing Various LVDS Issues

- High Temperature Deration

  LVDS drivers are outside the hot zone chamber area



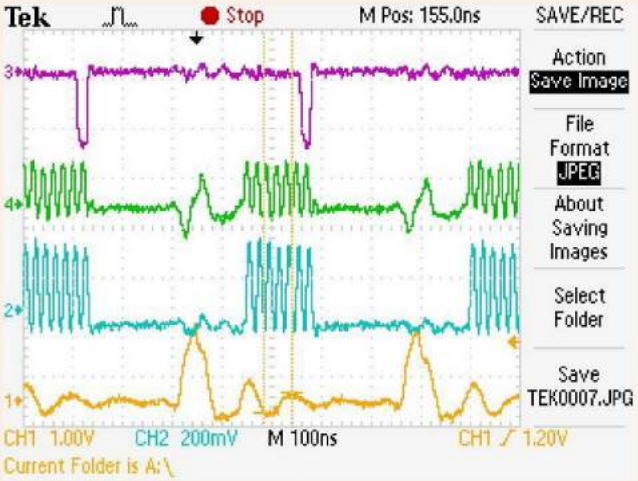
Design of Experiments

Objective:

- Check what is the maximum frequency that the LVDS set-up can generate

Design of Experiments

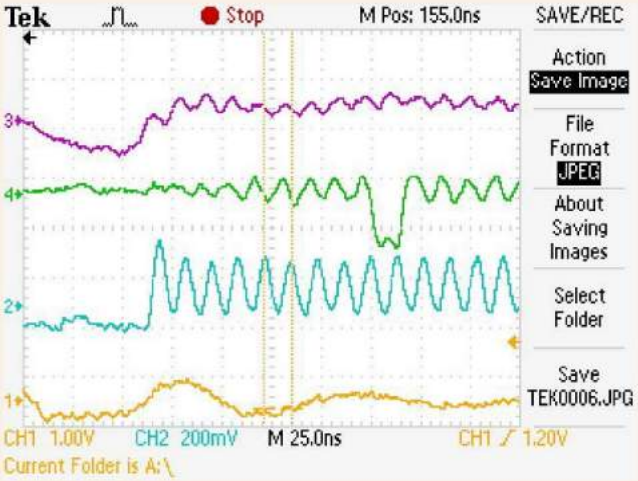
CLK+



LVDS Set-up at 50 MHz

Design of Experiments

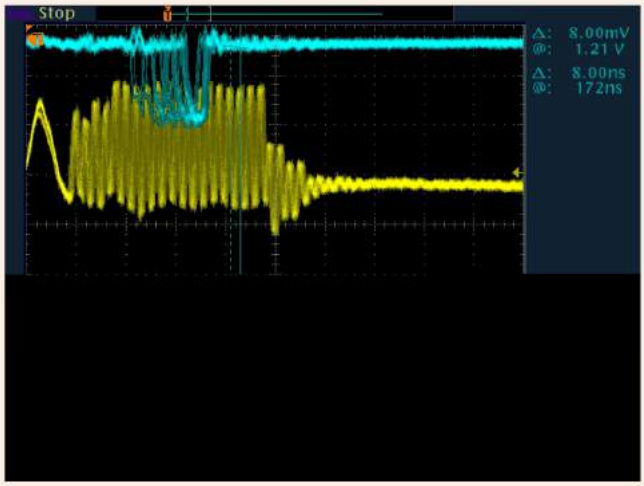
CLK+



LVDS Set-up at 75 MHz

Design of Experiments

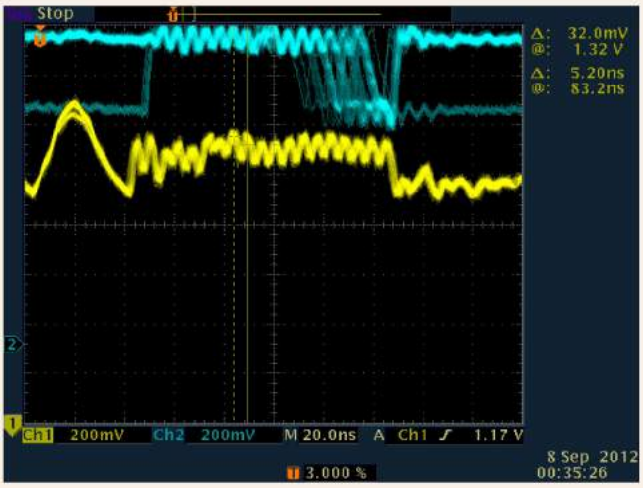
CLK+



LVDS Set-up at 125 MHz

Design of Experiments

CLK+



LVDS Set-up at 200 MHz

Results and Discussion

Frequency	Set-up Remarks
50Mhz	Passed
75Mhz	Passed
120Mhz	Passed
200Mhz	Frequency acquired but the levels are degraded

The LVDS Set-up can generate up to 200 MHz but the highest frequency achieved with good signal integrity is 120 MHz.

Recommendation

To achieve better results:

1) Further board developments
2) PCB CAD simulations
3) Bench Tests and Experiments
4) High RF Capability of Instruments
5) Avoid Edge Finger connections: Use high temp coax cables

Acknowledgement

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- **Eric Escalante, RF PCB Design Engineer,** for the guidelines and support to RF and LVDS designs.